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In the claims:

Following is a complete set of claims as amended with this Response.

1. (Currently Amended) A DSL system comprising:

a multiple loop segment, comprising K bonded loops, each loop comprising 2 wires, one of the 2K wires being selected as a reference wire, the remaining (2K-1) wires being referenced to the reference wire to provide up to (2K-1) communication channels, the (2K-1) channels using vectoring, the segment being coupled at one end to a plurality of different customer premises equipment (CPE) to provide different channels to different CPEs; and

a controller coupled to the multiple loop segment opposite the plurality of CPEs and configured to provide control signals used to operate the multiple loop segment as a vectored system by vectoring upstream and downstream transmissions with the plurality of CPEs across multiple active channels of the segment from the end of the multiple loop segment opposite the CPEs.

2. (Currently Amended) The DSL system of claim 1 wherein the controller comprises vectoring control means, the DSL system further comprising a customer vectoring unit (CVU) [[is]] coupled to a first end of the multiple loop segment and to the vectoring control means and a pedestal VU (PVU) [[is]] coupled to a second end of the multiple loop segment and to the vectoring control means for vectoring upstream and downstream transmissions across all active channels.

3. (Original) The DSL system of claim 2 wherein the PVU is in a pedestal and further wherein the CVU is in a customer premises.

4. (Original) The DSL system of claim 2 wherein the PVU is in a first pedestal and further wherein the CVU is in a second pedestal.

5. (Original) The DSL system of claim 2 wherein the PVU comprises a vector signal processing module coupled to the controller and further wherein the CVU comprises a vector signal processing module coupled to the controller.

6. (Original) The DSL system of claim 1 wherein at least one of the communication channels is operated using an expanded frequency spectrum.

7. (Previously Presented) The DSL system of claim 1 wherein the controller comprises means for controlling the frequency bandwidth used in transmitting data across the multiple loop segment.

8. (Original) The DSL system of claim 1 wherein the controller is a dynamic spectrum manager comprising vectoring control means comprising a computer system.

9. (Original) The DSL system of claim 1 wherein the controller comprises a computer system.

10. (Previously Presented) The DSL system of claim 1 further comprising a first impedance matching circuit coupled to a first end of the multiple loop segment and a second impedance matching circuit coupled to a second end of the multiple loop segment.

11. (Original) The DSL system of claim 1 wherein the DSL system is an ADSL system.

12. (Original) The DSL system of claim 1 wherein the DSL system is a VDSL system.

13. (Original) The DSL system of claim 1 wherein the loops are bonded using one of the following bonding protocols: TDIM bonding; Ethernet bonding; ATM bonding; or the G.bond protocol.

14. (Currently Amended) A DSL system comprising:

a multiple loop segment, each loop in the multiple loop segment having a pair of wires, the wires being connected so that at least two wires of the multiple bonded loops each carry a communication channel using a third wire of the multiple bonded loops as a common reference wire, the segment being coupled at one end to a plurality of different customer premises equipment (CPE) to provide different channels to different CPEs;

a first vectoring unit coupled to a first end of the multiple loop segment and comprising a first vector signal processing module the first vectoring unit being resident at one of a plurality of different CPEs;

a second vectoring unit coupled to a second end of the multiple loop segment opposite the plurality of CPEs and comprising a second vector signal processing module; and

wherein the first and second vectoring units are configured to provide vectored transmissions across the multiple loop segment, the second vectoring unit vectoring upstream and downstream transmissions with the plurality of CPEs across all active channels of the segment.

15. (Previously Presented) The DSL system of claim 14 wherein the controller is coupled to the first and second vectoring units, wherein the controller comprises vectoring control means, wherein the vectoring control means assists in regulating transmissions across the multiple loop segment.

16. (Original) The DSL system of claim 14 wherein the first vectoring unit is in a first pedestal and further wherein the second vectoring unit is in a second pedestal.

17. (Original) The DSL system of claim 14 wherein the first vectoring unit is in a customer premises and further wherein the second vectoring unit is in a pedestal.

18. (Original) The DSL system of claim 14 wherein the controller is a dynamic spectrum manager.

19. (Previously Presented) The DSL system of claim 14 wherein the controller further comprises frequency bandwidth control means for regulating the frequency bandwidth used in transmissions across the multiple loop segment.

20. (Previously Presented) The DSL system of claim 14 further comprising a first impedance matching circuit coupled to the first end of the multiple loop segment and a second impedance matching circuit coupled to the second end of the multiple loop segment.

21. (Currently Amended) A DSL system comprising:

a multiple loop segment, each loop in the multiple loop segment having a pair of wires, the wires being connected so that at least two wires of the multiple bonded loops each carry a communication channel using a third wire of the multiple bonded loops as a common reference wire, the segment being coupled at one end to a plurality of different customer premises equipments (CPE) to provide different channels to different CPEs;

a first impedance matching circuit coupled to a first end of the multiple loop segment;

a first vector signal processing module coupled to the first impedance matching circuit resident at one of the plurality of different CPEs;

a second impedance matching circuit coupled to a second end of the multiple loop segment;

a second vector signal processing module coupled to the second impedance matching circuit opposite the plurality of different CPEs; and

wherein the controller is coupled to the first and second vector signal processing modules and comprises:

means for collecting data regarding transmissions across the multiple loop segment; and

means for controlling vectoring of transmissions across the multiple loop segment so that the second vectoring unit vectors upstream and downstream transmissions with the plurality of CPEs across all active channels of the segment;

wherein the first and second vector signal processing modules are configured to process transmissions across the multiple loop segment.

22. (Previously Presented) The DSL system of claim 21 wherein the first and second vector signal processing modules provide two-sided vectoring of transmissions across the multiple loop segment.

23. (Previously Presented) The DSL system of claim 21 wherein the first and second vector signal processing modules provide one-sided vectoring of transmissions across the multiple loop segment.

24. (Previously Presented) The DSL system of claim 21 wherein the multiple loop segment couples customer premises equipment to a pedestal.

25. (Previously Presented) The system of claim 21 wherein the multiple loop segment couples a first pedestal to a second pedestal.

26. (Currently Amended) A method of sending high speed DSL signals through multiple communication channels comprising:

sending a first signal through a first communications channel to a first customer premises equipment (CPE) using a first wire of a first one of multiple bonded loops and a reference wire of a multiple loop segment;

sending a second signal through a second communications channel to a second CPE using a second wire of a second one of the multiple bonded loops of the multiple loop segment and the reference wire of the first channel, the common reference wire being a wire of a bonded loop of the multiple loop segment; and

vectoring upstream and downstream transmissions through the communications channels across the multiple loop segment across both communications channels from an upstream location.

27. (Currently Amended) The method of claim 26 wherein vectoring transmissions is performed using a first vectoring unit ~~and a second vectoring unit~~ coupled to ~~opposite ends of~~ the multiple loop segment opposite the CPEs.

28. (Previously Presented) The method of claim 26 wherein vectoring transmissions across the multiple loop segment comprises one-sided vectoring.

29. (Previously Presented) The method of claim 26 wherein vectoring transmissions across the multiple loop segment comprises two-sided vectoring.

30. (Previously Presented) The method of claim 26 wherein the vectored transmissions across the multiple loop segment utilize an expanded frequency spectrum on at least one channel.

31. (Previously Presented) The method of claim 26 further comprising providing vectoring control signals to the multiple loop segment.

32. (Previously Presented) The method of claim 31 wherein the vectoring control signals are provided by a dynamic spectrum manager.

33. (Currently Amended) The method of claim 31 wherein vectoring control signals are provided by [[is]] a DSM center.

34. (Previously Presented) The method of claim 31 wherein the vectoring control signals are provided by a computer system.

35. (Previously Presented) The method of claim 26 further wherein impedance matching circuits are provided at each end of the multiple loop segment.

36. (Previously Presented) The method of claim 26 wherein the loops are bonded using one of the following bonding protocols: TDIM bonding; Ethernet bonding; ATM bonding; or the G.bond protocol.

37. (New) The DSL system of claim 10, the first and second impedance matching circuits include a selected impedance placed between each wire and each other wire.

38. (New) The DSL system of claim 21, the first and second impedance matching circuits include a selected impedance placed between each wire and each other wire.